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For exclusive use of adopters of the book *Digital Design Principles and Practices*, Fourth Edition, by John F. Wakerly, ISBN 0-13-186389-4.

3e8.28 8.208 The maximum delay from clock to output of a 74HCT74 flip-flop is 44 ns. For a 4-bit ripple counter, the delay ripples through four such stages for a total maximum delay of 176 ns. Similarly, the maximum delays using 74AHCT and 74LS74 flip-flops are 40 ns and 160 ns, respectively.