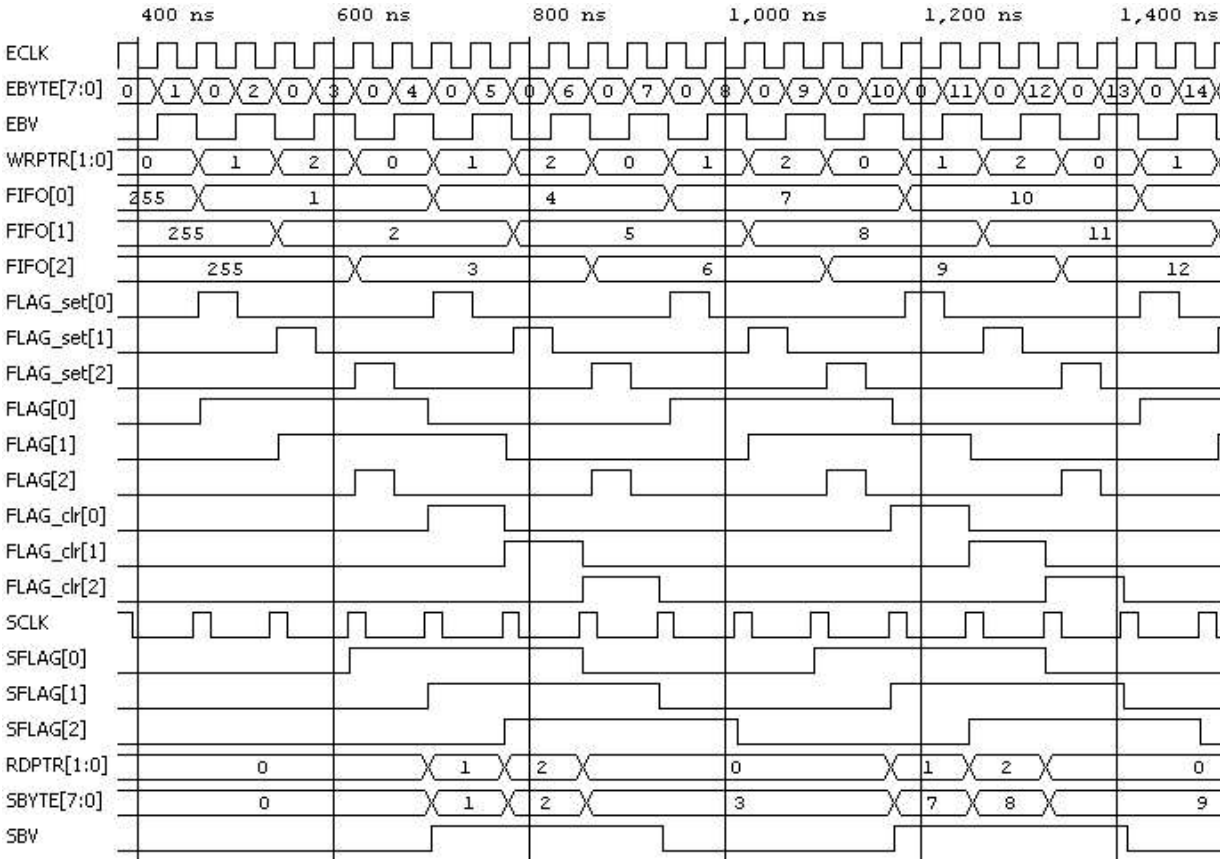

Figure 13-33 `VrEthSync` timing waveforms with `DEP=3` and slow SCLK.

resynthesize the design with parameter `DEP=2` and run the simulation, it still works. But we can't be complacent. We'd like our design to work even if `SCLK` is barely fast enough to keep up with the incoming Ethernet data rate, one byte every 80 ns. So, we can change the `SCLK` period in the test bench from 30 to 79 ns and see what happens. Not only does a FIFO depth of 2 no longer work, neither does 3, as shown in Figure 13-33. Here, `FLAG_set` for a particular FIFO location is being asserted before the `FLAG_clr` from its previous use has been negated. We need a depth of at least 4 for correct behavior, shown in Figure 13-34.

As the timing diagram in Figure 13-34 shows, once the first Ethernet output byte appears on `SBYTE`, they keep coming continuously. Further out, there is a 1-`SCLK`-tick gap at byte 35 and about every 80 `SCLK` ticks thereafter. This makes sense, since the `SCLK` period is just one part in 80 faster than the rate at which Ethernet input bytes arrive. Looking even further out in the simulation waveforms, the circuit continues to deliver Ethernet bytes on `SBYTE`, in order and with no omissions.